Remarks/Arguments

Claims 1-30 are pending in the present application. Claims 1 and 26 have been amended. Claims 27-30 have been added. The support for the amendment to claim 1 is found in pages 9-10 and elsewhere of the specification as filed. The support for new claims 27-30 is found on page 9, lines 9-27, of the specification as filed. It is respectfully submitted that no new matter has been added.

The Patent Office rejected claims 1 and 2 under 35 U.S.C. 103(a) as being unpatentable over Cox, "Subband Speech Coding and Matched Convolutional Channel Coding for Mobile Radio Channels."

Claim 1 recites "A communication unit for a multiple code rate communication system comprising a codeword defining N codeword elements and K information elements coded at a code rate R=K/(N-P), wherein P is a number of punctured elements of the codeword; a first storage location for storing an error reduction code mother code definition; **a second storage location for storing a maximum puncture sequence S_{max}, wherein S_{max} is the puncture sequence for a maximum code rate R_{max}, and further wherein S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1, wherein the codeword is one of decoded or encoded through the error reduction code mother code definition read from the first storage location and a selected one of S_1, S_2, ...S_{max} read from the second storage location, wherein the codeword is one of decoded or encoded through the error reduction code mother code definition read from the first storage location and a selected one of puncturing sequences S_1, S_2, ...S_{max} read from the second storage location.**"

The Patent Office asserted (pages 2-3 of the Office Action mailed January 12, 2006) "Cox discloses an encoder for generating framed (terminated) rate-compatible punctured convolutional codes (i.e., "error reduction codes"), the encoder being implemented by a programmable DSP. The terminated punctured convolutional codeword generated by Cox's encoder is a "codeword defining N codeword elements and K information elements coded at a code rate R=K/(N-P), wherein P is a number of punctured elements of the codeword." The processes of generating the mother code and of puncturing the mother code are shown by Cox as being performed in two separate stages (Figure 7), and the puncturing process is shown using a puncturing table that has a separate puncturing pattern for each rate. A region of DSP program memory with instructions for implementing the mother code encoding process shown by Cox apparently provides "a first storage location for storing an error reduction code mother code." A region of DSP memory for storing the puncturing process

table patterns shown by Cox for the highest rate rate-compatible puncturing scheme apparently provides "a second storage location for storing a maximum puncturing sequence Smax, wherein Smax is the puncture sequence for a maximum code rate Rmax, and further wherein Smax comprises a subset S1 that is a puncture sequence for a minimum code rate R1," here considering the "puncture sequence" to be the "0" bits, which are puncture pattern elements whose positions correspond (in the periodic application of the pattern) to positions of codeword bit to the punctured. In other words, **the "0" bits (i.e., the "puncture sequence") in Cox's puncturing patterns are positioned such that "the puncture sequence for a maximum code rate ... comprises a subset ... that is a puncture sequence for the maximum rate code," entirely because the puncturing is performed rate-compatibly. Accordingly, a subset (two) of Cox's (three) puncturing pattern a(1) bits that are "0" are present in puncturing pattern a(2), the third "0" in a(1), being replaced by a "1" in a (2).**"

"Regarding claim 1, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the rate-compatible punctured convolutional coding disclosed by Cox by using a "first storage location for storing an error reduction code mother code" and a "second storage location for storing a maximum puncturing sequence Smax, wherein S max is the puncture sequence for a maximum code rate Rmax, and further wherein Smax comprises a subset S1 that is a puncture sequence for a minimum code rate R1" because the process of generating the mother code and of puncturing the mother code as shown by Cox as being performed in two separate stages, and because the rate-compatible punctured convolutional coding disclosed by Cox is implemented by a processor with programmed instructions."

Cox appears to correspond to a prior art approach discussed in the background of the invention as an approach that may have substantial memory requirements (page 4, lines 2-9, of the application as filed). Cox (Figure 7) shows two 2X4 matrices, puncturing tables (page 1724, right hand column, two lines of text above equation 17 and line of text above equation 18) corresponding to puncturing rules a(1) and a(2), that provide two different code rates, 4/5 and 4/6. In Figure 7 of Cox, the two puncturing tables a(1) and a(2) are shown as distinct entities. These puncturing tables are of equal sizes, but hold different configurations of 0s and 1s. In Cox, "a zero in the puncturing table means that the code symbol is not to be transmitted," (page 1724, left hand column, lines 9-10 of the second paragraph). Cox appears to teach or at least fairly suggest that the two puncturing tables, corresponding to two matrices, have separate memory storage locations. Cox does not appear to disclose or fairly

suggest that the two matrices of the two rules correspond to a larger puncture sequence or that they are separable to form other puncture sequences or include a subset which represents a puncture sequence or to have any of the matrix values changed. There appears to be no disclosure of **a maximum puncture sequence Smax for a maximum code rate Rmax and a subset S1 of Smax which subset is for a minimum code rate R1**.

Furthermore, Cox does not appear to disclose or fairly suggest "the codeword is one of decoded or encoded through the error reduction code mother code definition read from the first storage location and a selected one of puncturing sequences S_1, S_2, ...S_{max} read from the second storage location."

Thus, claim 1 is allowable over Cox. Claim 2 is allowable over Cox because it depends from claim 1.

The Patent Office rejected claims 1-6 and 26 under 35 U.S.C. 103(a) as being unpatentable over Kim.

The Patent Office asserted (pages 4-5 of the Office Action mailed January 12, 2006) "Kim discloses an encoder for generating framed (terminated) rate-compatible punctured convolutional codes (which are "error reduction codes"). The terminated punctured codeword so generated is "a codeword defining N codeword elements and K information elements coded at a code rate R-K/(N-P) (*sic*), wherein P is a number of punctured elements of the codeword". The processes of generating the mother code (figure 1) and of subsequently puncturing the mother code (figure 2) are described by Kim as being performed in two separate stages. The puncturing process shown by Kim uses a puncturing table. A region of program memory with instructions for implementing the mother code encoding process shown by Kim would provide "a first storage location for storing an error reduction code mother code". A region of processor memory for storing the puncturing process table shown by Kim for the highest rate rate-compatible puncturing scheme would provide "a second storage location for storing a maximum puncturing sequence S_{max}, wherein S_{max} is the puncture sequence for a maximum code rate R_{max}, and further wherein S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1". Reference is hereby made to the relevant discussion of puncturing tables for rate-compatible codes, in the rejection citing Cox, above."

"Regarding claim 1, Official Notice is given that the convenience of implementing logic such as the logic in a channel coder by means of a processor with programmed instructions was well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement

the rate-compatible punctured convolutional coding disclosed by Kim by using a "first storage location for storing an error reduction code mother code" and a "second storage location for storing a maximum puncturing sequence S_{max}, wherein S_{max} is the puncture sequence for a maximum code rate R_{max}, and further wherein S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1" because the process of generating the mother code and of puncturing the mother code as shown by Kim as being performed in two separate stages, and because the convenience of implementing logic, such as the logic of a channel coder, by means of a processor with programmed instructions was already well known."

The Patent Office asserted "The puncturing process shown by Kim uses a puncturing table. A region of program memory with instructions for implementing the mother code encoding process shown by Kim would provide "a first storage location for storing an error reduction code mother code". A region of processor memory for storing the puncturing process table shown by Kim for the highest rate rate-compatible puncturing scheme would provide "a second storage location for storing a maximum puncturing sequence S_{max}, wherein S_{max} is the puncture sequence for a maximum code rate R_{max}, and further wherein S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1"

Kim shows (Figure 2, page 2401) examples of a puncturing table for Rate Compatible Punctured Serial Concatenated Convolutional Codes. Kim discloses (page 2400, right hand column, last nine lines) "For each puncturing index k_S, we define an n_I x P binary puncturing table, PT_k, wherein puncturing index $k_S = 0, 1, \ldots, (n_I - 1)P$ that can be set according to channel conditions. For systematic puncturing PT_0 must contain P ones in the first row. PT_{ks+1} must have ones in the same positions as PT_k, plus an additional one and, finally, $PT_{(nI-1)P}$ becomes a puncturing table of all ones." Kim does not disclose that the individual puncturing tables are able to be concatenated or subdivided or have any of their matrix values changed. Instead, as shown in Figure 2, puncturing table PT0 corresponds to coding rate 2/3, PT1 to coding rate 8/15, PT2 to coding rate 4/9, PT3 to coding rate 8/21, and PT4 to coding rate 1/3. Like Cox, Kim appears to be directed to a prior art approach discussed in the background of the invention as an approach that may have substantial memory requirements (page 4, lines 2-9, of the application as filed). Kim does not appear to disclose or fairly suggest **a maximum puncture sequence S_{max}, wherein S_{max} is the puncture sequence for a maximum code rate R_{max}, and further wherein S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1.**

Furthermore, Kim does not appear to disclose or fairly suggest "the codeword is one of decoded or encoded through the error reduction code mother code definition read from the first storage location and a selected one of puncturing sequences S_1, S_2, ...S_{max} read from the second storage location."

Thus, claims 1-6 and 26 are allowable over Kim.

The taking of Official Notice "that the convenience of implementing logic such as the logic in a channel coder by means of a processor with programmed instructions was well known at the time the invention was made" by the Patent Office is challenged. The Patent Office is requested to provide a reference supporting the material and motivation asserted as part of the Official Notice in the paragraph at the top of page 5 of the Office Action mailed January 12, 2006. Applicant is unsure why Official Notice was taken in light of the language of Applicant's own claims 1-6 and 26 and Kim.

As to claim 4, Kim does not teach or suggest subsets. Thus, Kim does not make obvious claim 4.

As to claims 5 and 6, Kim discloses puncture table entries (Figure 2) that each contain the same number of bits as other entries and does not make obvious either claim 5 or claim 6.

The Patent Office rejected claims 1, 2, 4-10, and 20-25 under 35 U.S.C. 103(a) as being unpatentable over Mantha, U.S. Published Patent Application No. 2003/0126551.

Claim 1 recites "A communication unit for a multiple code rate communication system comprising a codeword defining N codeword elements and K information elements coded at a code rate R=K/(N-P), wherein P is a number of punctured elements of the codeword; a first storage location for storing an error reduction code mother code definition; a second storage location for storing a maximum puncture sequence S_{max}, wherein **S_{max} is the puncture sequence for a maximum code rate R_{max},** and further wherein **S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1, wherein the codeword is one of decoded or encoded through the error reduction code mother code** definition read from the first storage location and a selected one of puncturing sequences S_1, S_2, ...S_{max} read from **the second storage location.**"

Claim 20 recites "A transmitter comprising an information source for providing a codeword; **a memory for storing a low density parity check code LDPC mother code definition** and a maximum puncture sequence S_{max}; a LDPC encoder having an input coupled to an output of the information source and an input coupled to an output of the memory; and a modulator having an input coupled to an output of the LDPC encoder, wherein the encoder operates in one instance to encode at a maximum rate R_{max} by puncturing elements of a

codeword in locations described by **the maximum puncture sequence S_{max} read from the memory**, and in another instance to encode at a lesser rate R_1 by puncturing elements of a codeword in locations described by **a subset S_1 of the maximum puncture sequence S_{max} read from the memory**."

Claim 23 recites "A receiver comprising a demodulator for demodulating a received codeword; **a memory for storing a low density parity check code LDPC mother code definition** and a maximum puncture sequence S_{max}; and a LDPC decoder having an input coupled to an output of the demodulator and an input coupled to an output of the memory; wherein the decoder operates in one instance to decode at a maximum rate R_{max} by de-puncturing elements of a codeword in locations described by **the maximum puncture sequence S_{max} read from the memory**, and in another instance to decode at a lesser rate R_1 by de-puncturing elements of a codeword in locations described by **a subset S_1 of the maximum puncture sequence S_{max} read from the memory**."

The Patent Office asserted (page 6 of the Office Action mailed January 12, 2006) "Mantha discloses an encoder for generating rate-compatibly punctured LDPCs, implemented by software. Each punctured LDPC codeword so generated is "a codeword defining N codeword elements and K information elements coded at a code rate R-K/(N-P), wherein P is a number of punctured elements of the codeword." The processes of generating the mother code (figure 1) and of subsequently puncturing the mother code (figure 2) are described by Mantha as being performed in two separate stages. Mantha describes the use of a puncturing table as "typical" [0136] and instead uses an algorithm based on two parameters in order to generate the puncturing patterns. Because the codes are punctured rate-compatibly, the puncturing patterns used by Mantha must be such that "S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1" [0127]."

"Regarding claim 1, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement the rate-compatible punctured LDPC encoding and decoding disclosed by Mantha by using a "first storage location for storing an error reduction code mother code" and a "second storage location for storing a maximum puncturing sequence S_{max}" because the process of generating the mother code and of puncturing the mother code are shown by Kim as being performed separately, because Kim teaches the use of puncturing tables storing puncturing sequences to be "typical," and because the encoder and decoder are implemented by software. A region of memory with instructions for implementing the mother code encoding process shown by Mantha would provide "a first storage location for storing an error reduction code mother code" and a region of processor

memory for storing the puncturing process table shown by Mantha for the highest rate rate-compatible puncturing scheme would provide a "second storage location for storing a maximum puncturing sequence S_{max}".

Mantha (paragraph 0127) discloses "FIGS. 13 and 14 show serially concatenated systems. In FIG. 13, each new parity block P_1 is generated from the previously transmitted parity block P_{i-1} except of course P_1 , which is generated from the systematic information bits directly. All encoders 134a-134d and decoders 136a-136d can be identical. They can implement either turbo codes or LDPC codes. In FIG. 14 however, new parity blocks are generated in encoders 144a-144d from all previously transmitted bits. By using all previously transmitted bits, the code performance will improve, provided that the decoders 146a-performance [sic]. Additionally, any puncturing strategy must meet rate compatibility requirements. This means that at any particular code rate generated by puncturing, the parity bits involved must also be used by any lower rate code that might also be generated by puncturing."

Mantha discloses (regarding figure 1, paragraph 0059) "FIG. 1 depicts the type of channel considered in this disclosure. It is a discrete, memoryless channel. A discrete channel is defined as a system consisting of an input alphabet X and output alphabet Y and a probability transition matrix p(x|y) that represents the probability of observing the output symbol y given that the symbol x is transmitted. The channel is said to be memoryless if the probability distribution of the output depends only on the input at that time and is conditionally independent of previous channel inputs or outputs. These assumptions are justified because most modem communication systems operate on the basis of discrete symbol values."

Mantha, in paragraph 0136, discloses "An advantage to arbitrary puncturing is that a puncture mask for any puncturing amount can completely be described with just two numbers, the increment value δ and the initial value of the accumulator, σ_1 in FIG. 16. This means that the transmitter can inform the receiver (or vice versa) of the puncturing amount and hence code rate with a minimal exchange of information. This is in contrast with typical applications of puncturing, where the puncturing amounts are predetermined and stored in a lookup table in both the transmitter and the receiver." (Presumably, Kim represents a typical application.)

Mantha teaches using an accumulator with selectable increments to determine the parity bits for puncturing (paragraphs 0129-0132). Mantha teaches that selected parity bits are selected by an increment value's being added in an accumulator such that when the

accumulator overflows the current parity bit value is selected for transmission (paragraph 0130) and that when the accumulator process is over, the selected parity bits are transmitted (paragraph 0132). Mantha does not seem to disclose "S_{max} comprises a subset S_1 that is a puncture sequence for a minimum code rate R_1," "a subset S_1 of the maximum puncture sequence S_{max}," or "**a subset S_1 of the maximum puncture sequence S_{max} read from the memory**." Kim does not disclose a subset that is a puncture sequence for a minimum code rate, a subset of the maximum puncture sequence, or that the subset of the maximum puncture sequence is read from the memory. None of Kim, Cox, or Mantha disclose or fairly suggest **a subset S_1 of the maximum puncture sequence S_{max} read from the memory** or **a selected one of puncturing sequences S_1, S_2, ...S_{max} read from the second storage location**. In Kim and Cox, there is no disclosure or fair suggestion of a subset of a maximum puncture sequence. In Mantha, the selected parity bits are derived through use of an accumulator with all the parity bits, but any selected parity bits are not read from the memory or a second storage location.

As to claims 4-6, the Patent Office asserted (page 7 of the Office Action mailed January 12, 2006) "Regarding claims 4-6, 21, 22, 24, and 25, Mantha shows [0142] six different code rates, with the codes collectively meeting the recited puncturing limitations." Mantha does not seem to teach or suggest subsets. As to claim 4, Mantha does not appear to teach or fairly suggest "S_{max} further comprises at least two subsets S_i that are puncture sequences for code rates R_i, wherein i is an integer greater than or equal to one and each sequentially higher i^{th} code rate is higher than the sequentially lower i^{th} code rate." As to claims 5 and 6, Kim discloses puncture table entries (Figure 2) that each contain the same number of bits as other entries. As to claim 5, Mantha does not disclose or fairly suggest "each S_i comprises at least one memory element, and each S_i with at least two memory elements has at least one memory element in common with another S_i and with S_{max}." As to claims 22 and 25, Mantha does not disclose or fairly suggest "each of S_1, S_2 and S_3 are subsets of S_{max} but not subsets of any of the other of S_1, S_2 and S_3." As to claim 6, Mantha does not disclose or fairly suggest "$S_1 \subseteq S_2 \subseteq \ldots \subseteq S_{max-1} \subseteq S_{max}$." Thus, Mantha does not make obvious claims 4-6, 22, or 25.

The Patent Office asserted (page 7 of the Office Action mailed January 12, 2006) "Regarding claims 20 and 23, Mantha's encoder and decoder of course require a modulator and demodulator and apparently are envisaged for a transceiver with software for encoding and decoding sharing the same program memory." As for claim 20, Mantha does not appear

to disclose or fairly suggest "wherein the encoder operates in one instance to encode at a maximum rate R_{max} by puncturing elements of a codeword in locations described by the **maximum puncture sequence S_{max} read from the memory**, and in another instance to encode at a lesser rate R_1 by puncturing elements of a codeword in locations described by **a subset S_1 of the maximum puncture sequence S_{max} read from the memory**." As for claim 23, Mantha does not appear to disclose or fairly suggest "wherein the decoder operates in one instance to decode at a maximum rate R_{max} by de-puncturing elements of a codeword in locations described by **the maximum puncture sequence S_{max} read from the memory**, and in another instance to decode at a lesser rate R_1 by de-puncturing elements of a codeword in locations described by **a subset S_1 of the maximum puncture sequence S_{max} read from the memory**." Thus, claims 20 and 23 are allowable.

The Patent Office asserted (page 7 of the Office Action mailed on January 12, 2006) "Regarding claims 4-6, 21, 22, 24, and 25, Mantha shows [0142] six different code rates, with the codes collectively meeting the recited puncturing limitations." As for claim 21, Mantha does not appear to disclose or fairly suggest "the encoder encodes at any of rates R_{max}, R_3, R_2, and R_1 by puncturing elements of a codeword in locations described by the respective sequences S_{max}, S_3, S_2, and S_1, wherein $R_{max}>R_3>R_2>R_1$ and $S_1 \subseteq S_2 \subseteq S_3 \subseteq S_{max}$." As to claim 22, Mantha does not appear to disclose or fairly suggest "the encoder encodes at any of rates R_{max}, R_3, R_2, and R_1 by puncturing elements of a codeword in locations described by the respective sequences S_{max}, S_3, S_2, and S_1, wherein $R_{max}>R_3>R_2>R_1$ and each of S_1, S_2 and S_3 are subsets of S_{max} but not subsets of any of the other of S_1, S_2 and S_3." As to claim 24, Mantha does not appear to disclose or fairly suggest "the decoder decodes at any of rates R_{max}, R_3, R_2, and R_1 by de-puncturing elements of a codeword in locations described by the respective sequences S_{max}, S_3, S_2, and S_1, wherein $R_{max}>R_3>R_2>R_1$ and $S_1 \subseteq S_2 \subseteq S_3 \subseteq S_{max}$." As to claim 25, Mantha does not appear to disclose or fairly suggest "the decoder decodes at any of rates R_{max}, R_3, R_2, and R_1 by de-puncturing elements of a codeword in locations described by the respective sequences S_{max}, S_3, S_2, and S_1, wherein $R_{max}>R_3>R_2>R_1$ and each of S_1, S_2 and S_3 are subsets of S_{max} but not subsets of any of the other of S_1, S_2 and S_3." Thus, claims 21, 22, 24, and 25 are not made obvious by Mantha.

The Patent Office asserted (page 8 of the Office Action mailed January 12, 2006) "Regarding claim 26, each bit of the separate puncturing patterns that would be used in a typical arrangement based on puncturing tables would be presumably be stored in a "memory element" (i.e., storage location) and each different pattern would presumably not share

common storage locations with other patterns." Mantha does not disclose or fairly suggest "each S_i comprises at least one memory element, and there is at least one S_i that has no memory elements in common with another S_i." Thus, claim 26 is not made obvious by Mantha.

New claims 27-30 are believed to be allowable over the prior art of record.

The Applicant respectfully requests that the Patent Office review the cited art and rejections in light of the above remarks, and pass each of claims 1-26 to issue. The undersigned representative welcomes the opportunity to resolve any matters that may remain, formal or otherwise, via teleconference at the Patent Office's discretion.

Thus, claims 1, 2, 4-10, and 20-26 are allowable over Mantha, alone or in combination with Kim.

Regarding the remarks on page 8 of the Office Action mailed January 12, 2006, "Applicant describes the maximum puncture sequence as "represented by a relatively long sequence of memory elements 54, which are depicted as sequential but need not be stored in physically adjacent areas of a volatile memory. A first puncture sequence S_1 is stored at a first memory element 54a, which is the first memory element of the sequence of memory elements that comprise the maximum rate puncture sequence S_{N-K}. In terms of matrix H of Figure 1A. A second puncture sequence S_2 is stored at a first 54a and second 54b memory elements, which are the first two memory elements of the sequence of memory elements that comprise the maximum rate puncture sequence S_{N-K}" however the rejected claims are of course not necessarily specific to such a storage scheme, as explained in the rejections. Applicant observes that "S_1 is a subset of S_2, which is a subset of S_3, etc., and all are subsets of S_{N-K}. This relation is written as $S_1 \subseteq S_2 \subseteq S_3 \subseteq \ldots \subseteq S_{N-K}$." The examiner has demonstrated that the same property of subsets applies to the positions of puncture-indicating values (e.g. the positions of Cox's "0"s) in any set of rate compatible puncturing patterns."

Claims 1-10 and 20-30 all recite that the maximum puncture sequence and a subset of the maximum puncture sequence are read from memory or a storage location. In Mantha, the parity bits are punctured at regular intervals as determined through the use of an accumulator and determinable increment value that allows parity bits to be selected regularly. Cox and Kim both disclose tables that appear to have fixed lengths. None of Mantha, Cox, and Kim disclose that the subset S_1 is read from memory. Thus, claims 1-10 and 20-29 are allowable for this and other reasons as discussed above.

The Patent Office asserted (page 9 of the Office Action mailed January 12, 2006) "Regarding Kim, applicant writes "only a single rate encoder and decoder is used for variable

coding rates, this statement is seen to apply to both the inner and outer encoder separately, so both the transmitter and the receiver each use an inner and separate outer encoder/decoder separately, so both the transmitter and the receiver each user an inner and separate outer encoder/decoder to achieve the variable rate codes. Were it otherwise, the code would not be concatenated. The two encoders/decoders are not seen as combinable with ordinary skill because the outer code is interleaved prior to application of the inner code." The rejection based on Kim argues that a software implementation of Kim's logic is obvious, which applicant's arguments do not address. Kim's two encoders and decoders are already combined, thus applicant's argument is not coherent."

"As applicant does not accurately represent the Official Notice actually given in the rejection citing Kim, i.e. simply that the advantages of using software (instead of hardwired logic) to perform logic operations were already well known, applicant's requests for references supporting Official Notice not taken are presumed unintentional. The examiner here asserts the factual basis of the Official Notice is already evident to any practitioner by the disclosure of Cox."

Applicant continues to request a reference corresponding to the subject matter that Official Notice was taken. It is believed that the currently pending claims patentably define over Mantha, Cox, and Kim, alone or in combination.

The Patent Office asserted (pages 9-10 of the Office Action mailed January 12, 2006) "As should be clear from the present Office actions discussion of Cox's well-known approach of using a puncture table with separate entries for each rate of a rate-compatible code combined with the understanding that the rejections based on Kim and Mantha cite the same well-known approach, the characterization that "the Office Action appears to rely on Kim's description of a puncturing table, shared by the transmitter and receiver, as teaching that the puncturing table is used to achieve a maximum code rate and a subset of (the puncture table) is used to achieve a minimum code rate" is incorrect. Each puncturing pattern relied on by the rejections, whether referred to as a single table entry or as one table of a plurality of tables, has been shown to meet the claim limitations simply as a result of being one of a set of rate-compatible puncturing patterns."

With the amendment of claim 1, all pending claims 1-10 and 20-29 recite that the maximum puncture sequence S_{max} and subsets of Smax, such as S1 and Si, are read from memory. Applicant believes that this claim feature defines over Mantha, Cox, and Kim.

Claims 7-9 are allowable because they depend from allowable base claims.

Respectfully submitted:

Walter J. Malinowski
Reg. No.: 43,423

March 22, 2006
Date

Customer No.: 29683
HARRINGTON & SMITH, LLP
4 Research Drive
Shelton, CT 06484-6212
Phone: (203) 925-9400, extension 19
Facsimile: (203) 944-0245
Email: wmalinowski@hspatent.com

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